REMARKS

Claims 9 and 15 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. The applicant respectfully submits that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **June 29, 2005**.

Claim Rejections under 35 USC §103

Claims 8-13, 15 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. (US 6,417,575 B2) in view of Lee et al. (US 6,163,074).

The present invention is a semiconductor device having a pad capable of suppressing excess current concentration. As illustrated in Fig. 2a, the pad includes a large number of insulating regions (21a) in which specific ratios of dimensions are followed. For example, W1 corresponds to the width of the wiring portion (25). The pad is divided into three portions. A first frame area (27a) having a width of L1. A second frame area (27c) has a width L2 and contains several insulating regions (21a). A central area (27d) is contained in the middle of the pad and may contain a via hole. The width L1 of the first frame area (27 a) is equal to or wider than the distance between insulating regions (21a). As illustrated in Fig. 2A, the total width of pad (27) corresponds to 2 x W2 + n x W3 as discussed on page 11, line 22 of the specification, W1 correspond to the distance L1 and W3

corresponds to the distance P2. As discussed in the example provided on page 12, lines 4-11, W1 is larger than the distance L1 and the ratio L1/W1 is 30 percent or higher.

Harada et al. describes a semiconductor device and method of manufacturing the same which includes a pad electrode and main electrode layer. This device includes a first interlayer insulating film (7) a first intra-layer insulating film (11). Please note that the pad portion of this device is wider than the wiring portion.

Lee et al. describes a semiconductor device having a lower single-bodied conductive plug (930) and a lower island insulator (925I) as shown in figures 9 and 10. With this design a bonding pad having reduced cracking in an insulating layer is possible.

In the Preliminary Amendment submitted on June 13, 2005, the limitation that upper surfaces of the first pad, the wiring and the insulating regions are on a same level was added to claim 9, and the limitation that upper surfaces of the first pad and the insulating regions are on a same level was added to claim 15. Regarding these newly added limitations, the Examiner cites embodiments shown in Figs. 74B, 75B and 85B of Harada, which were not cited in the previous Office Actions. The Examiner states that the insulating regions (301, 321, 331 and 341 in Fig. 85B) have an upper surface that is same level as the upper surface of the pad (101) and he wiring part (300) in the Response to Arguments on page 5 of the Office Action.

Applicant does not agree with the Examiner.

In Fig. 74B of Harada, the upper surface of the insulating regions 321 is not the same level as that of the pad 101. The upper surface of the insulating region 331 and the pad 250 seem to have

the same level. However, the region 330 is not a pad, but a stress buffer metal layer (column 32, lines 25-27). As shown in Fig. 74A, the stress buffer metal layer 330 is separated from the pad 250. Therefore, the insulating region 331 is located outside of the pad 250. In contrast, the claimed insulating regions are disposed on the bottom of the pad part. Namely, the insulating regions are located inside of the pad part. The insulating region 331 of Harada is definitely distinguished from the insulating regions of claims 9 and 15.

The insulating regions 331, 321 and 301 shown in Fig. 75B of Harada are also located outside of the pad parts 250 and 251. The insulating regions 341, 331, 321 and 301 shown in Fig. 85B of Harada are also located outside of the pad parts 250 and 251.

As described above, Harada does not disclose insulating regions which are disposed on the bottom of the pad part and have upper surfaces that are the same level as the upper surface of the pad.

To overcome the rejection, Claims 9 and 15 have been amended to include the limitation that the first pad contained in the pad part of the recess has a continuous body.

Therefore, independent claims 9 and 15 patentably distinguish over the prior art relied upon, by reciting, as exemplified by claim 9,

> "A semiconductor device comprising: a semiconductor substrate; a first interlayer insulating film made of insulating material and formed on the semiconductor substrate; a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part, a plurality of insulating regions disposed on the bottom of the pad part, and the recess being formed so that

> the insulating regions are not disposed in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width but disposed in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width; a first pad filled in the pad part of the recess; and a wiring filled in the wiring part of the recess, wherein upper surfaces of said first pad, said wiring and said insulating regions are on a same level, wherein said first pad contained in said pad part of said recess has a continuous body." (Emphasis Added)

Regarding claim 12, the Examiner states "Lee et al. shows (Fig. 18) an alternate embodiment where a plurality of insulating regions (9251 or 9451) are disposed regularly and have a first pitch (space between the insulting regions). As seen from the drawings, the width of the first frame area (width between lines of outer periphery of pad 960 and outer periphery of the first outside insulating region 9451) is wider than the first pitch of the insulating regions."

It appears that the Examiner believes that the first pitch is defined by the space between the insulating regions. However, the Examiner's understanding is incorrect. The first pitch is defined by the distance P shown in Fig. 2A of the present application. The first pitch is not equal to the distance P2.

Furthermore, it appears that the Examiner believes that the outer periphery of the pad is defined by the outer periphery of the pad 960. However, the Examiner's understanding is incorrect. In claim 12, the upper surface of the pad and the upper surface of the insulating regions have the same level. As shown in Figs. 9 and 10 of Lee, the pad 960 is located above the upper surface of the insulating regions 9451. In Fig. 18 of Lee, the pad, the upper surface of which is the same level of the upper surface of the insulating regions 9451, corresponds to the region indicated by the reference

number 950'. In the pattern shown in Fig. 18 of Lee, which is attached, the width of the first frame area is undoubtedly narrower than the first pitch.

Therefore, withdrawal of the rejection of Claims 8-13, 15 and 20 under 35 U.S.C. 103(a) as being unpatentable over Harada et al. (US 6,417,575 B2) in view of Lee et al. (US 6,163,074) is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, the claims, as amended, are believed to be patentable and in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosure: Fig. 18 of Lee et al. (USP 6,163,074)

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